DATA SHEET

SAA6579
Radio Data System (RDS) demodulator

Product specification
Supersedes data of 1997 Feb 24
File under Integrated Circuits, IC01

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Philips
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Radio Data System (RDS) demodulator SAA6579

FEATURES

- Anti-aliasing filter (2nd order)
- Integrated 57 kHz band-pass filter (8th order)
- Reconstruction filter (2nd order)
- Clocked comparator with automatic offset compensation
- 57 kHz carrier regeneration
- Synchronous demodulator for 57 kHz modulated RDS signals
- Selectable 4.332/8.664 MHz crystal oscillator with variable dividers
- Clock regeneration with lock on biphase data rate
- Biphase symbol decoder with integrate and dump functions
- Differential decoder
- Signal quality detector
- Subcarrier output.

GENERAL DESCRIPTION

The integrated CMOS circuit SAA6579 is an RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting.

The data signal RDDA and the clock signal RDCL are provided as outputs for further processing by a suitable decoder (microcomputer).

The operational functions of the device are in accordance with the *"CENELEC EN 50067"*.

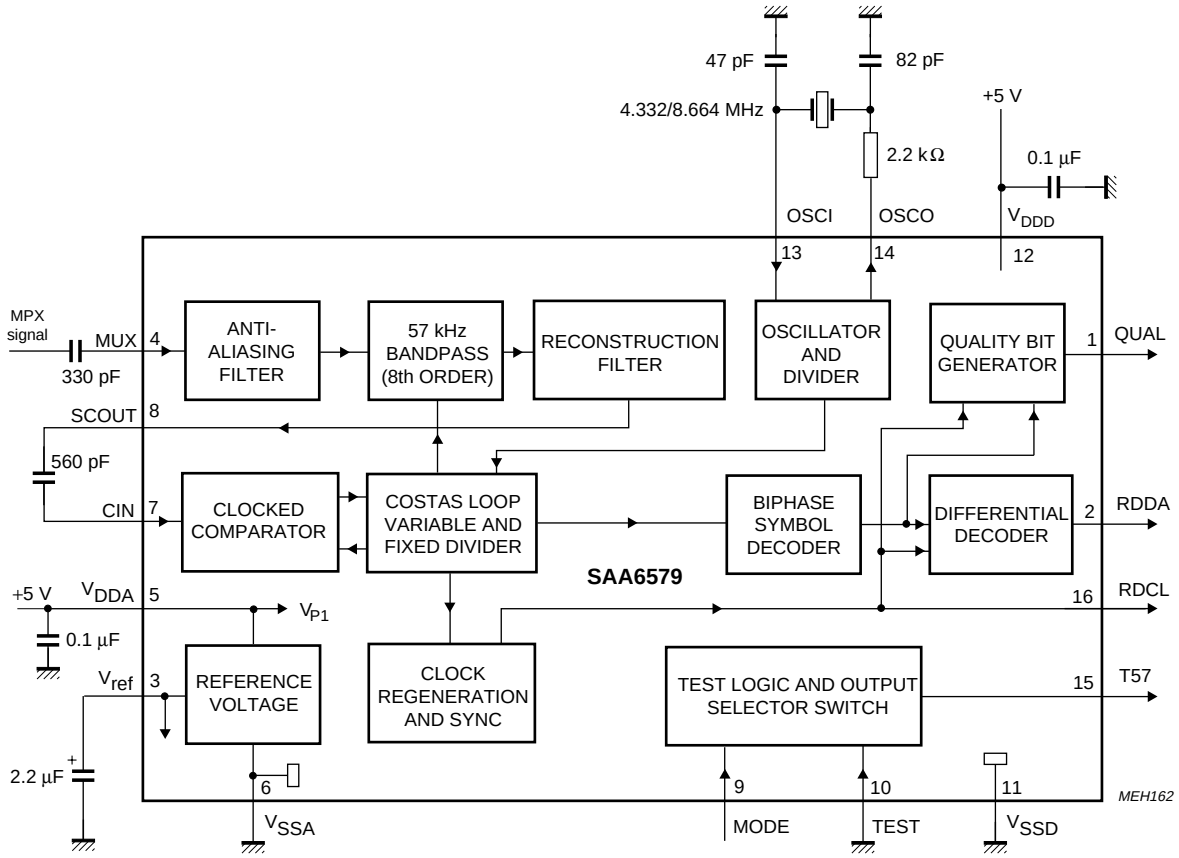
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	3.6	5.0	5.5	V
V_{DDD}	digital supply voltage (pin 12)	3.6	5.0	5.5	V
I_{tot}	total supply current	–	6	–	mA
$V_{i(rms)}$	RDS input amplitude (RMS value; pin 4)	1	–	–	mV
V_{OH}	HIGH-level output voltage for signals RDDA, RDCL, QUAL and T57	4.4	–	–	V
V_{OL}	LOW-level output voltage for signals RDDA, RDCL, QUAL and T57	–	–	0.4	V
T_{amb}	operating ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6579	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
SAA6579T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM



Via pin MODE two different crystal frequencies can be used.

MODE	CRYSTAL CLOCK
LOW	4.332 MHz
HIGH	8.664 MHz

Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
QUAL	1	quality indication output
RDDA	2	RDS data output
V_{ref}	3	reference voltage output ($0.5V_{DDA}$)
MUX	4	multiplex signal input
V_{DDA}	5	+5 V supply voltage for analog part
V_{SSA}	6	ground for analog part (0 V)
CIN	7	subcarrier input to comparator
SCOUT	8	subcarrier output of reconstruction filter
MODE	9	oscillator mode/test control input
TEST	10	test enable input
V_{SSD}	11	ground for digital part (0 V)
V_{DDD}	12	+5 V supply voltage for digital part
OSCI	13	oscillator input
OSCO	14	oscillator output
T57	15	57 kHz clock signal output
RDCL	16	RDS clock output

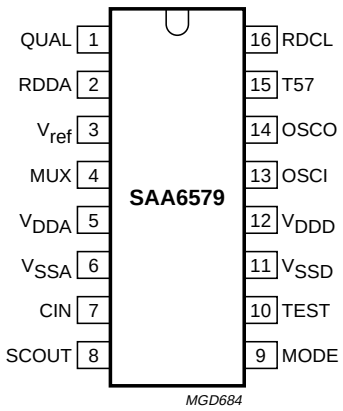


Fig.2 Pin configuration.

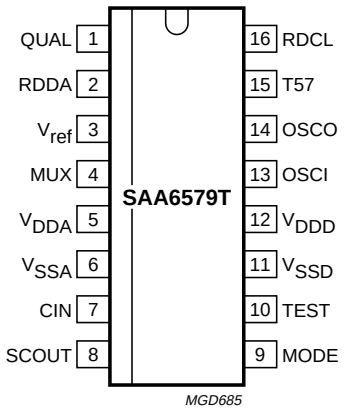


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); ground pins 6 and 11 connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		0	6	V
V_{DDD}	digital supply voltage (pin 12)		0	6	V
V_n	voltage on all pins; grounds excluded		–0.5	V_{DDX} + 0.5	V
T_{stg}	storage temperature		–40	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling for all pins except pins 9 and 10	note 1	±300	–	V
		note 2	+1500	–3000	V

Notes

1. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

FUNCTIONAL DESCRIPTION

The SAA6579 is a demodulator circuit for RDS applications. It contains a 57 kHz bandpass filter and a digital demodulator to regenerate the RDS data stream out of the multiplex signal (MPX).

Filter part

The MUX signal is band-limited by a second-order anti-aliasing-filter and fed through a 57 kHz band-pass filter (8th order band-pass filter with 3 kHz bandwidth) to separate the RDS signals. This filter uses switched capacitor technique and is clocked by a clock frequency of 541.5 kHz derived from the 4.332/8.664 MHz crystal oscillator. Then the signal is fed to the reconstruction filter to smooth the sampled and filtered RDS signal before it is output on pin 8. The signal is AC-coupled to the comparator (pin 7). The comparator is clocked with a frequency of 228 kHz (synchronized by the 57 kHz of the demodulator).

Digital part

The synchronous demodulator (Costas loop circuit) with carrier regeneration demodulates the internal coupled, digitized signal. The suppressed carrier is recovered from the two sidebands (Costas loop). The demodulated signal is low-pass-filtered in such a way that the overall pulse shape (transmitter and receiver) approaches a cosinusoidal form in conjunction with the following Integrate and dump circuit.

The data-spectrum shaping is split into two equal parts and handled in the transmitter and in the receiver. Ideally, the data filtering should be equal in both of these parts.

The overall data-channel-spectrum shaping of the transmitter and the receiver is approximately 100% roll-off.

The integrate and dump circuit performs an integration over a clock period. This results in a demodulated and valid RDS signal in form of biphase symbols being output from the integrate and dump circuit. The final stages of RDS data processing are the biphase symbol decoding and the differential decoding. After synchronization by data clock RDCL (pin 16) data appears on the RDDA output (pin 2). The output of the biphase symbol decoder is evaluated by a special circuit to provide an indication of good data (QUAL = HIGH) or corrupt data (QUAL = LOW).

Timing

Fixed and variable dividers are applied to the 4.332/8.664 MHz crystal oscillator to generate the 1.1875 kHz RDS clock RDCL, which is synchronized by the incoming data. Which ever clock edge is considered (positive or negative going edge) the data will remain valid for 399 μs after the clock transition. The timing of data change is 4 μs before a clock change. Which clock transition (positive or negative going clock) the data change occurs in, depends on the lock conditions and is arbitrary (bit slip).

During poor reception it is possible that faults in phase occur, then the clock signal stays uninterrupted, and data is constant for 1.5 clock periods. Normally, faults in phase do not occur on a cyclic basis. If however, faults in phase occur in this way, the minimum spacing between two possible faults in phase depends on the data being transmitted. The minimum spacing cannot be less than 16 clock periods. The quality bit changes only at the time of a data change.

CHARACTERISTICS

V_{DDA} = V_{DDD} = 5 V; T_{amb} = 25 °C and measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		3.6	5.0	5.5	V
V_{DDD}	digital supply voltage (pin 12)		3.6	5.0	5.5	V
I_{tot}	total supply current	$I_5 + I_{12}$	–	6	–	mA
V_{ref}	reference voltage (pin 3)	V_{DDA} = 5 V	–	2.5	–	V
MPX input (signal before the capacitor on pin 4)						
$V_{i\ MPX(rms)}$	RDS amplitude (RMS value)	$\Delta f = \pm 1.2$ kHz RDS; $\Delta f = \pm 3.5$ kHz ARI; see Fig.5	1	–	–	mV
$V_{i\ MPX(p-p)}$	maximum input signal capability (peak-to-peak value)	f = 57 ±2 kHz	200	–	–	mV
		f < 50 kHz	1.4	–	–	V
		f < 15 kHz	2.8	–	–	V
		f > 70 kHz	3.5	–	–	V
R_{4-6}	input resistance	f = 0 to 100 kHz	40	–	–	kΩ
G_{8-4}	signal gain	f = 57 kHz	17	20	23	dB
57 kHz band-pass filter						
f_c	centre frequency	T_{amb} = –40 to +85 °C	56.5	57.0	57.5	kHz
B	–3 dB bandwidth		2.5	3.0	3.5	kHz
G	stop band gain	$\Delta f = \pm 7$ kHz	31	–	–	dB
		f < 45 kHz	40	–	–	dB
		f < 20 kHz	50	–	–	dB
		f > 70 kHz	40	–	–	dB
$R_{o(8)}$	output resistance (pin 8)	f = 57 kHz	–	26	–	Ω
Comparator input (pin 7)						
$V_{i(rms)}$	minimum input level (RMS value)	f = 57 kHz	–	1	10	mV
R_i	input resistance		70	110	150	kΩ
Oscillator input (pin 13)						
V_{IH}	HIGH-level input voltage	V_{DDD} = 5.0 V	4.0	–	–	V
V_{IL}	LOW-level input voltage	V_{DDD} = 5.0 V	–	–	1.0	V
I_I	input current	V_{DDD} = 5.5 V	–	–	±1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital demodulator and outputs QUAL, RDDA, T57, OSCO and RDCL (pins 1, 2, 14, 15 and 16)						
V_{OH}	HIGH-level output voltage	I_Q = –20 µA; V_{DDD} = 4.5 V	4.4	–	–	V
V_{OL}	LOW-level output voltage	I_Q = 3.2 mA; V_{DDD} = 5.5 V	–	–	0.4	V
f_{RDCL}	nominal clock frequency RDCL		–	1187.5	–	Hz
Δt_{RDCL}	jitter of RDCL		–	–	18	µs
f_{T57}	nominal subcarrier frequency T57	note 1	–	57.0	–	kHz
I_O	output current OSCO (pin 14)	V_{DDD} = 4.5 V; V_{14} = 0.4 V	1.5	–	–	mA
		V_{DDD} = 4.5 V; V_{14} = 4.1 V	–1.6	–	–	mA
	output current QUAL, RDDA, T57, RDCL (pins 1, 2, 15 and 16)	V_{DDD} = 4.5 V; V_O = 0.4 V	3.0	–	–	mA
		V_{DDD} = 4.5 V; V_O = 4.1 V	–3.0	–	–	mA
4.332 MHz crystal parameters						
f_0	XTAL frequency		–	4.332	–	MHz
Δf_{max}	maximum permitted tolerance		–	±50	–	10^{-6}
Δf_o	adjustment tolerance of f_0	T_{amb} = 25 °C	–	–	±20	10^{-6}
		T_{amb} = –40 to +85 °C	–	–	±25	10^{-6}
C_L	load capacitance		–	30	–	pF
R_{xtal}	resonance resistance		–	–	60	Ω
8.664 MHz crystal parameters						
f_0	XTAL frequency		–	8.664	–	MHz
Δf_{max}	maximum permitted tolerance		–	±50	–	10^{-6}
Δf_o	adjustment tolerance of f_0	T_{amb} = 25 °C	–	–	±30	10^{-6}
		T_{amb} = –40 to +85 °C	–	–	±30	10^{-6}
C_L	load capacitance		–	30	–	pF
R_{xtal}	resonance resistance		–	–	60	Ω

Note

1. The signal T57 has a phase lead of 123° (±180°) relative to the ARI carrier at output SCOUT.

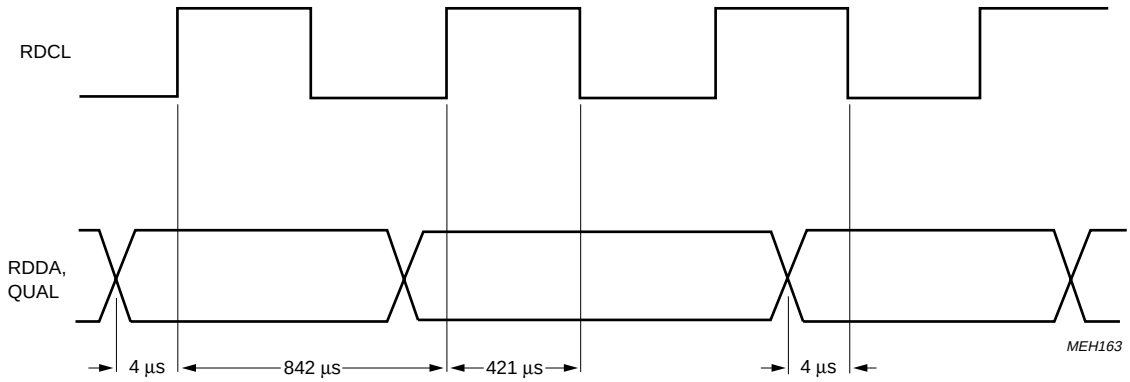
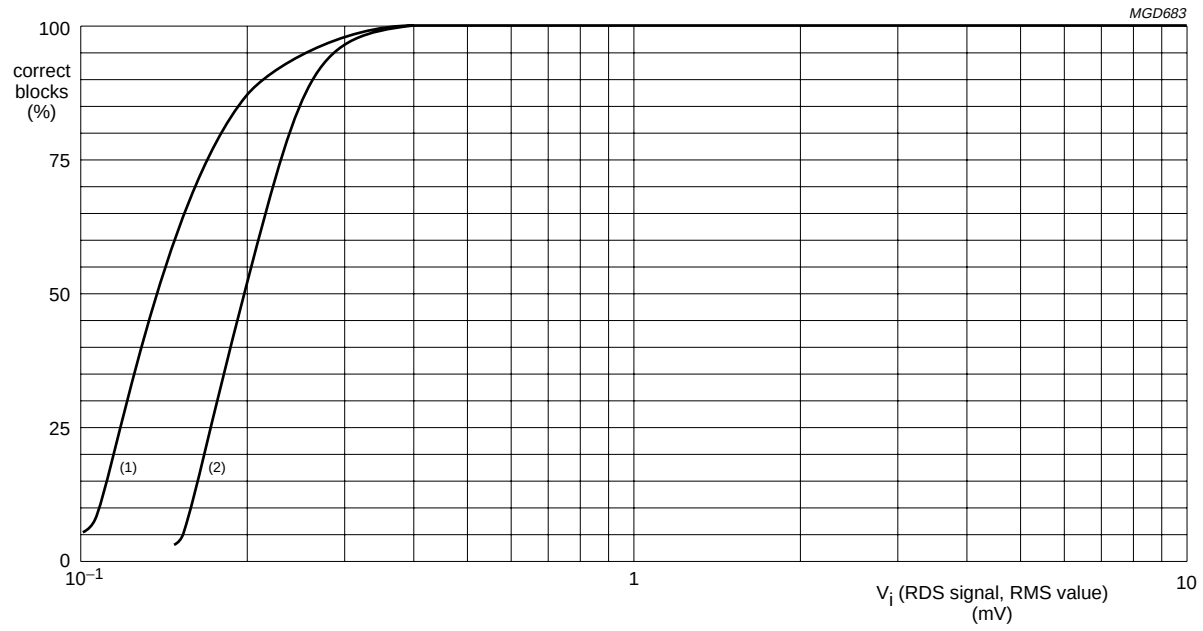


Fig.4 RDS timing diagram including a phase jump.

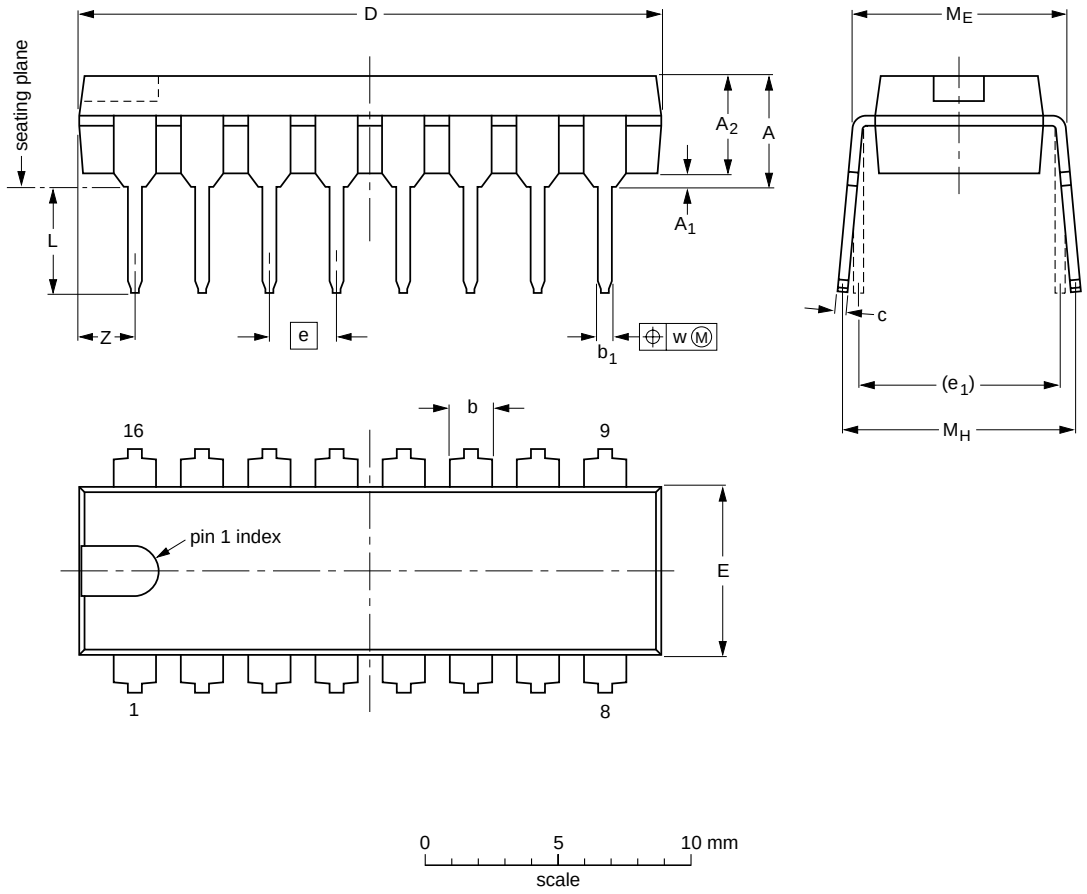


(1) RDS + ARI (BK).
(2) RDS only.

Fig.5 Typical RDS sensitivity.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

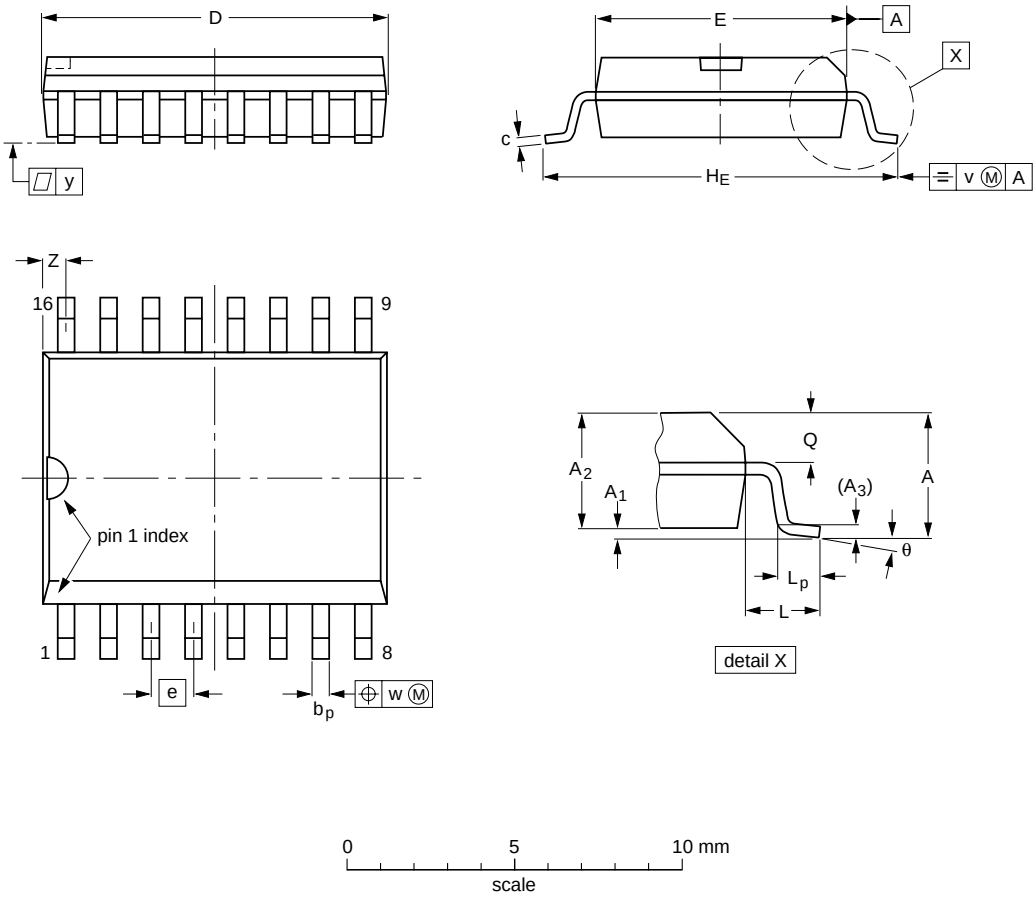
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001	SC-503-16			~~95-01-19~~ 99-12-27

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				~~97-05-22~~ 99-12-27

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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